Tankeblue

Silicon Carbide Substrates

（Version:2021）

Product Specifications

4H N-Type
4H Semi-insulating

Prepare/Date :　　**Check/Date** :　　**Approve/Date** :

SILICON CARBIDE MATERIAL PROPERTIES※

Property	4H-SiC, Single Crystal
Lattice Parameters	a=3.076 Å c=10.053 Å
Stacking Sequence	ABCB
Mohs Hardness	≈9.2
Density	3.21 g/cm^3
Therm. Expansion Coefficient	4-5×10^{-6}/K
Refraction Index @750nm	n_o = 2.61 n_e = 2.66
Dielectric Constant	c~9.66
Thermal Conductivity (N-type, 0.02 ohm.cm)	a~4.2 W/cm·K@298K c~3.7 W/cm·K@298K
Thermal Conductivity (Semi-insulating)	a~4.9 W/cm·K@298K c~3.9 W/cm·K@298K
Band-Gap	3.23 eV
Break-Down Electrical Field	3-5×10^{6}V/cm
Saturation Drift Velocity	2.0×10^{5}m/s

※ Silicon carbide material properties is only for reference.

APPLICATIONS

III-V Nitride Deposition

Optoelectronic Devices

High-Power Devices

High-Temperature Devices

High-Frequency Power Devices

GENERAL DEFINITION

WA4CDE-XXX

W – Standard

A – Diameter
- 2 – 50.8 mm (2 inch)
- 4 – 100.0 mm (4 inch)
- 6 – 150.0 mm (6 inch)

4 – 4H-SiC

C – Dopant
- N – Nitrogen
- S – Semi-insulating

D –Orientation
- 0 – On-axis
- 4 – 4° off axis

E – Grade
- Z – Zero MPD
- P – Product
- D – Dummy

X– Silicon face polish
- L – Lapping
- P – Optical polish
- C – CMP, EPI-ready

X – Carbon face polish
- L – Lapping
- P – Optical polish
- C – CMP, EPI-ready

X – Thickness
- E – 350 µm
- F – 330 µm
- B – 500 µm
- X – Other thickness

PRODUCT DESCRIPTIONS

Silicon Carbide (SiC) Substrate Orientation	
SURFACE ORIENTATION	The tilt angle between the crystallographic c-axis and vector normal to wafer surface (see Figure 1).
ORTHOGONAL MISORIENTATION	In {0001} wafers intentionally cut “off axis”, the angle between the projection of the surface normal onto a {0001} plane and the nearest $<11\bar{2}0>$ direction.
OFF AXIS (FOR 4H-N)	4.0° toward $<11\bar{2}0>\pm0.5°$
ON AXIS (FOR 4H-SI)	<0001>±0.5°

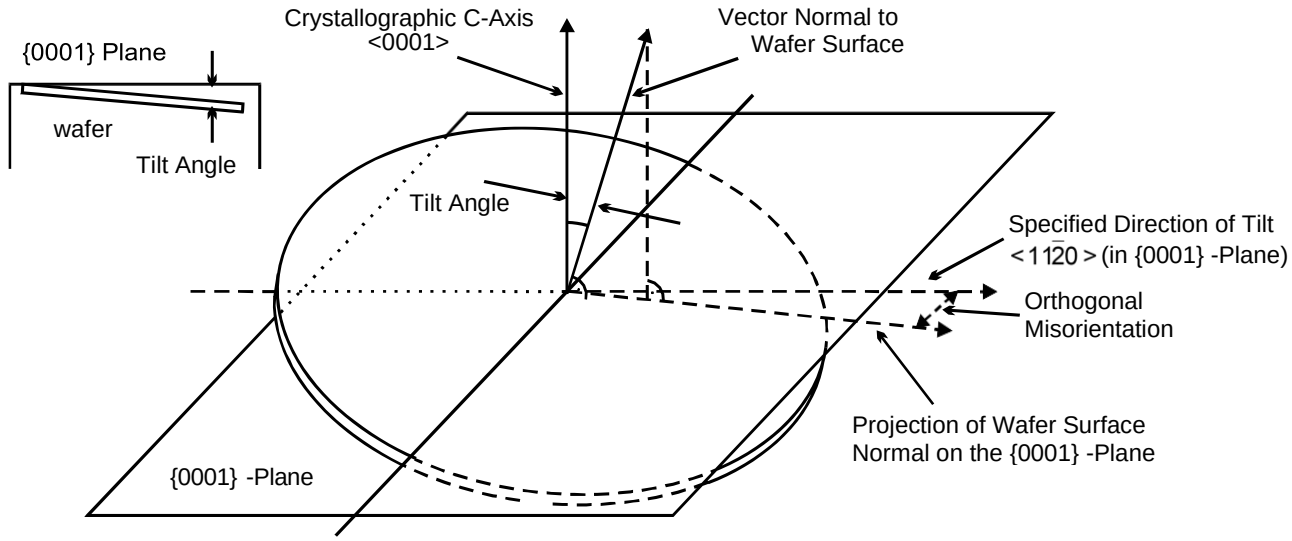

Figure. 1 Orthogonal Misorientation

4H N-TYPE SIC SUBSTRATE

WAFER DIAMETER	The linear dimension across the surface of a wafer. Measure the diameter of wafer with qualified digital caliper (see Figure 2 and 3).
PRIMARY FLAT	The flat of the longest length on the wafer, whose crystal surface is parallel with the $\{10\bar{1}0\}$ lattice plane.
PRIMARY FLAT ORIENTATION	The primary flat orientation is always parallel to the $<11\bar{2}0>$ direction (or, which is the same, parallel to the $\{10\bar{1}0\}$ lattice plane). Measured with XRD back reflection technique.
SECONDARY FLAT	A flat of shorter length than the primary flat, whose position with respect to the primary flat identifies the face of the wafer. Not applicable to 150mm wafers (see Figure 3).
SECONDARY FLAT ORIENTATION	Silicon face up: The secondary flat orientation is 90˚ clockwise from the primary flat.
MARKING	For silicon-face polished material, the carbon face of each individual wafer is laser-marked with OCR-compatible font (see Figure 2 and 3).

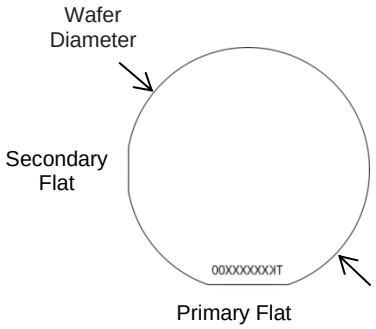

Figure.2 Diameter, primary and secondary flat locations and marking orientation of 100mm SiC wafer (4H-N) (silicon face up for SiC).

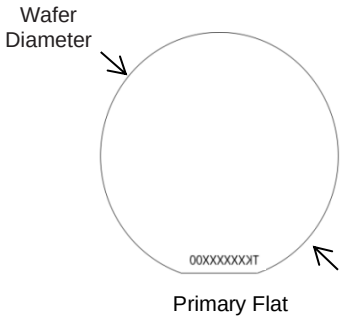

Figure.3 Diameter, primary flat locations and marking orientation of 150mm SiC wafer (4H-N) (silicon face up for SiC).

4H SEMI-INSULATING SIC SUBSTRATE

WAFER DIAMETER	The linear dimension across the surface of a wafer. Measure the diameter of wafer with qualified digital caliper (see Figure 4 and 5).
PRIMARY FLAT	The flat of the longest length on the wafer, whose crystal surface is parallel with the $\{10\bar{1}0\}$ lattice plane. Not applicable to 150mm wafers.
PRIMARY FLAT ORIENTATION	The primary flat orientation is always parallel to the $<11\bar{2}0>$ direction (or, which is the same, parallel to the $\{10\bar{1}0\}$ lattice plane). Measured with XRD back reflection technique.
SECONDARY FLAT	A flat of shorter length than the primary flat, whose position with respect to the primary flat identifies the face of the wafer. Not applicable to 150mm wafers.
SECONDARY FLAT ORIENTATION	Silicon face up: The secondary flat orientation is 90˚ clockwise from the primary flat.
NOTCH	All 150mm (4H-SI) products have a notch with 1.0~1.25mm depth. The laser markings are offset right when looking at the carbon face (see Figure 5).
MARKING	For silicon-face polished material, the carbon face of each individual wafer is laser-marked with OCR-compatible font (see Figure 4 and 5).

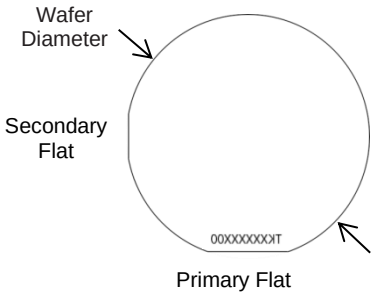

Figure.4 Diameter, primary and secondary flat locations and marking orientation of 100mm SiC wafer (4H-SI) (silicon face up for SiC).

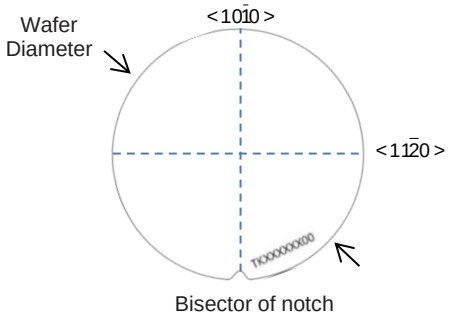

Figure.5 Notch location and marking orientation of 150 mm wafers (4H-SI) (carbon face up for SiC).

天科合达 6 英寸 SiC 晶片产品标准

6 inch diameter Silicon Carbide (SiC) Substrate Specification

等级Grade			精选级（Z 级）Zero MPD Production Grade	工业级（P 级）Standard Production Grade (P Grade)	测试级（D 级）Dummy Grade (D Grade)
直径	Diameter		149.5 mm~150.0 mm		
厚度	Thickness	4H-N	350 μm±20 μm	350 μm±25 μm	
		4H-SI	500 μm±20 μm	500 μm±25 μm	
晶片方向	Wafer Orientation		Off axis: 4.0° toward <11$\bar{2}$0>±0.5° for 4H-N, On axis: <0001>±0.5° for 4H-SI		
微管密度※	Micropipe Density	4H-N	≤0.5 cm^{-2}	≤2 cm^{-2}	≤15cm^{-2}
		4H-SI	≤1 cm^{-2}	≤5 cm^{-2}	≤15cm^{-2}
电阻率※	Resistivity	4H-N	0.015~0.025 Ω·cm		0.015~0.028 Ω·cm
		4H-SI	≥1E9 Ω·cm		≥1E5 Ω·cm
主定位边方向	Primary Flat Orientation		{10-10} ±5.0°		
主定位边长度	Primary Flat Length	4H-N	47.5 mm±2.0 mm		
		4H-SI	Notch		
边缘去除	Edge Exclusion		3 mm		
局部厚度变化/总厚度变化/弯曲度/翘曲度 LTV/TTV/Bow /Warp			≤3 μm/≤6 μm/≤30 μm/≤40 μm		≤5 μm/≤15 μm/≤40 μm/≤60 μm
表面粗糙度※	Roughness		Polish Ra≤1 nm		
			CMP Ra≤0.2 nm		Ra≤0.5 nm
边缘裂纹 (强光灯观测) Edge Cracks By High Intensity Light			None		Cumulative length ≤ 20 mm, single length≤2 mm
六方空洞 (强光灯观测) ※ Hex Plates By High Intensity Light			Cumulative area ≤0.05%		Cumulative area ≤0.1%
多型 (强光灯观测) ※Polytype Areas By High Intensity Light			None		Cumulative area≤3%
目测包裹物 (日光灯下观测) Visual Carbon Inclusions			Cumulative area ≤0.05%		Cumulative area ≤3%
划痕 (强光灯观测)# Silicon Surface Scratches By High Intensity Light			None		Cumulative length≤1×wafer diameter
崩边 (强光灯观测) Edge Chips By High Intensity Light			None permitted ≥0.2mm width and depth		5 allowed, ≤1 mm each
硅面污染物 (强光灯观测) Silicon Surface Contamination by High Intensity Light			None		
包装	Packaging		Multi-wafer Cassette or Single Wafer Container		

Notes:

※Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

天科合达 4 英寸 SiC 晶片产品标准

4 inch diameter Silicon Carbide (SiC) Substrate Specification

等级Grade			精选级（Z 级）Zero MPD Production Grade (Z Grade)	工业级（P 级）Standard Production Grade (P Grade)	测试级（D 级）Dummy Grade (D Grade)
直径	Diameter		99.5 mm~100.0 mm		
厚度	Thickness	4H-N	350 μm±20 μm	350 μm±25 μm	
		4H-SI	500 μm±20 μm	500 μm±25 μm	
晶片方向	Wafer Orientation		Off axis: 4.0° toward $<11\bar{2}0>$ ±0.5° for 4H-N, On axis: <0001>±0.5° for 4H-SI		
微管密度※	Micropipe Density	4H-N	≤0.5cm^{-2}	≤2 cm^{-2}	≤15 cm^{-2}
		4H-SI	≤1cm^{-2}	≤5 cm^{-2}	≤15 cm^{-2}
电阻率※	Resistivity	4H-N	0.015~0.025 Ω·cm		0.015~0.028 Ω·cm
		4H-SI	≥1E9 Ω·cm		≥1E5 Ω·cm
主定位边方向	Primary Flat Orientation		{10-10} ±5.0°		
主定位边长度	Primary Flat Length		32.5 mm±2.0 mm		
次定位边长度	Secondary Flat Length		18.0 mm±2.0 mm		
次定位边方向	Secondary Flat Orientation		Silicon face up: 90° CW. from Prime flat ±5.0°		
边缘去除	Edge Exclusion		3 mm		
局部厚度变化/总厚度变化/弯曲度/翘曲度	LTV/TTV/Bow /Warp		≤3 μm/≤5 μm/≤15 μm/≤30 μm		≤10 μm/≤15 μm/≤25 μm/≤40 μm
表面粗糙度※	Roughness		Polish Ra≤1 nm		
			CMP Ra≤0.2 nm		Ra≤0.5 nm
边缘裂纹 (强光灯观测)	Edge Cracks By High Intensity Light		None		Cumulative length ≤ 10 mm, single length≤2 mm
六方空洞 (强光灯测) ※	Hex Plates By High Intensity Light		Cumulative area ≤0.05%		Cumulative area ≤0.1%
多型 (强光灯观测) ※	Polytype Areas By High Intensity Light		None		Cumulative area≤3%
目测包裹物 (日光灯观测)	Visual Carbon Inclusions		Cumulative area ≤0.05%		Cumulative area ≤3%
硅面划痕 (强光灯观测) #	Silicon Surface Scratches By High Intensity Light		None		Cumulative len`gth≤1×wafer diameter
崩边 (强光灯观测)	Edge Chips High By Intensity Light		None permitted ≥0.2 mm width and depth		5 allowed, ≤1 mm each
硅面污染物 (强光灯观测)	Silicon Surface Contamination By High Intensity		None		
包装	Packaging		Multi-wafer Cassette or Single Wafer Container		

Notes:

※ Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.